CLAIMS

1. A digital differential input receiver circuit, comprising:

an input receiver having first and second input terminals and at least one output terminal, the input receiver being operable to receive a signal at the first input terminal from an input/output terminal;

a reference voltage source coupled to apply a reference voltage to the second input terminal;

an isolation circuit coupled between the input/output terminal and the reference voltage source, the isolation circuit being operable to isolate the input/output terminal from the reference voltage source responsive to an activation signal; and

an output signal detector operable to detect an output signal applied to the input/output terminal and to generate the activation signal responsive thereto.

2. The digital differential input receiver circuit of claim 1 wherein the isolation circuit is coupled between the second input terminal of the input receiver and the reference voltage source.

3. The digital differential input receiver circuit of claim 1 wherein the isolation circuit is coupled between the input/output terminal and the first input terminal of the input receiver.

4. The digital differential input receiver circuit of claim 1 wherein the isolation circuit comprises a first pass gate coupled between the input/output terminal and the reference voltage source, the pass gate being operable responsive to the activation signal.

5. The digital differential input receiver circuit of claim 4, further comprising:

a dummy load; and

a second pass gate, the second pass gate being coupled between the input/output terminal and the dummy load.

6. The digital differential input receiver circuit of claim 5 wherein the dummy load comprises a circuit substantially identical to the input receiver.

7. The digital differential input receiver circuit of claim 1 wherein the input receiver includes a pair of differential transistors coupled to each other through a common node, and wherein the isolation circuit comprises a bias circuit operable responsive to the activate signal to bias the differential transistors to a non-linear operating range.

8. The digital differential input receiver circuit of claim 7 wherein the bias circuit is coupled to the common node of the input receiver.

9. The digital differential input receiver circuit of claim 1 wherein the output signal detector comprises a logic gate.

10. The digital differential input receiver circuit of claim 9 wherein the logic gate comprises a NOR gate.

11. A digital differential input receiver, comprising:

input receiver means having first and second input terminals and at least one output terminal;

first coupling means for coupling a signal from an input/output terminal to the first input terminal of the input receiver means;

reference voltage means for generating a reference voltage;

second coupling means for coupling the reference voltage to the second input terminal of the input receiver means;

isolation means coupled between the input/output terminal and the reference voltage means, the isolation means isolating the input/output terminal from the reference voltage means responsive to an activation signal; and

output signal detector means for detecting an output signal applied to the input/output terminal and for generating the activation signal responsive thereto.

12. The digital differential input receiver of claim 11 wherein the isolation means is coupled between the second input terminal of the input receiver means and the reference voltage means.

13. The digital differential input receiver of claim 11 wherein the isolation means is coupled between the input/output terminal and the first input terminal of the input receiver means.

14. The digital differential input receiver of claim 11, further comprising:

dummy load means; and

means for coupling the input/output terminal to the dummy load when the output signal detector means detects an output signal being applied to the input/output terminal.

15. The digital differential input receiver of claim 11, wherein the isolation means comprises bias means for biasing the input receiver means to a non-linear operating range responsive to the activate signal.

16. A memory device, comprising:

a memory array having a plurality of memory cells arranged in rows and columns;

a reference voltage source coupled to generate a reference voltage;

an address decoder coupled to receive a plurality of address signals through respective address terminals, the address signals designating a location in the memory array to

be accessed, the address decoder including a plurality of input receivers each having a first input coupled to a respective address terminal and a second input coupled to receive the reference voltage from the reference source;

a command decoder coupled to receive memory command and generate control signals corresponding thereto;

a data output buffer coupled to receive data signals from the memory array, the data output buffer receiving respective data signals and applying the data signals to respective data terminals; and

a data input buffer coupled to apply data signals to the memory array, the data input buffer comprising:

a plurality of input receivers each having respective output terminal coupled to the memory array, each input receiver having a first input coupled to a respective one of the data terminals and a second input terminal coupled to receive the reference voltage from the reference source;

a plurality of isolation circuits coupled between a respective one of the data terminals and the reference voltage source, the isolation circuit being operable to isolate the respective data terminal from the reference voltage source responsive to a respective activation signal; and

a plurality of output signal detectors each operable to detect an output signal applied to a respective one of the data terminals by the data output buffer.

17. The memory device of claim 16, wherein the data output buffer comprises a plurality of output drivers each coupled to a respective one of the data terminals to apply respective data signals to the respective data terminals.

18. The memory device of claim 17, wherein each of the output drivers generates a respective output enable signal when the output driver is applying an output signal to the respective data terminal.

19. The memory device of claim 18, wherein each of the output signal detectors is operable to detect a respective output enable signal from a respective output driver and to generate a respective one of the activation signals responsive thereto.

20. The memory device of claim 16 wherein each of the isolation circuits is coupled between the second input terminal of a respective input receiver and the reference voltage source.

21. The memory device of claim 16 wherein each of the isolation circuits is coupled between a respective one of the data terminals and the first input terminal of a respective input receiver.

22. The memory device of claim 16 wherein each of the isolation circuits comprises a first pass gate coupled between a respective one of the data terminals and the reference voltage source, the pass gate being operable responsive to a respective one of the activation signals.

23. The memory device of claim 22 bias the differential transistors to a non-linear operating range, wherein each isolation circuit further comprises:

a dummy load; and

a second pass gate, the second pass gate being coupled between the respective data terminal and the dummy load.

24. The memory device of claim 23 wherein each of the dummy loads comprises a circuit substantially identical to a respective one of the input receivers.

25. The memory device of claim 16 wherein each of the input receivers comprises a pair of differential transistors coupled to each other through a common node, and wherein each of the isolation circuits comprises a respective bias circuit operable responsive

to a respective one of the activate signals to bias the differential transistors to a non-linear operating range.

26. The memory device of claim 25 wherein each of the bias circuits is coupled to the common node of the respective input receiver.

27. The memory device of claim 16 wherein each of the output signal detectors comprises a respective logic gate.

28. The memory device of claim 27 wherein the logic gate comprises a NOR gate.

29. A computer system comprising:

a processor;

a system controller coupled to the processor;

a peripheral device bus coupled to the processor through the system controller;

an input device coupled to the peripheral device bus;

an output device coupled to the peripheral device bus;

a mass storage device coupled to the peripheral device bus; and

a memory device coupled to the processor through the system controller, the memory device comprising:

a memory array having a plurality of memory cells arranged in rows and columns;

a reference voltage source coupled to generate a reference voltage;

an address decoder coupled to receive a plurality of address signals through respective address terminals, the address signals designating a location in the memory array to be accessed, the address decoder including a plurality of input receivers each having a first input coupled to a respective address terminal and a second input coupled to receive the reference voltage from the reference source;

a command decoder coupled to receive memory command and generate control signals corresponding thereto;

a data output buffer coupled to receive data signals from the memory array, the data output buffer receiving respective data signals and applying the data signals to respective data terminals; and

a data input buffer coupled to apply data signals to the memory array, the data input buffer comprising:

a plurality of input receivers each having respective output terminal coupled to the memory array, each input receiver having a first input coupled to a respective one of the data terminals and a second input terminal coupled to receive the reference voltage from the reference source;

a plurality of isolation circuits coupled between a respective one of the data terminals and the reference voltage source, the isolation circuit being operable to isolate the respective data terminal from the reference voltage source responsive to a respective activation signal; and

a plurality of output signal detectors each operable to detect an output signal applied to a respective one of the data terminals by the data output buffer.

30. The computer system of claim 29 wherein the data output buffer comprises a plurality of output drivers each coupled to a respective one of the data terminals to apply respective data signals to the respective data terminals.

31. The computer system of claim 30 wherein each of the output drivers generates a respective output enable signal when the output driver is applying an output signal to the respective data terminal.

32. The computer system of claim 31 wherein each of the output signal detectors is operable to detect a respective output enable signal from a respective output driver and to generate a respective one of the activation signals responsive thereto.

33. The computer system of claim 29 wherein each of the isolation circuits is coupled between the second input terminal of a respective input receiver and the reference voltage source.

34. The computer system of claim 29 wherein each of the isolation circuits is coupled between a respective one of the data terminals and the first input terminal of a respective input receiver.

35. The computer system of claim 29 wherein each of the isolation circuits comprises a first pass gate coupled between a respective one of the data terminals and the reference voltage source, the pass gate being operable responsive to a respective one of the activation signals.

36. The computer system of claim 35 wherein each isolation circuit further comprises:

a dummy load; and

a second pass gate, the second pass gate being coupled between the respective data terminal and the dummy load.

37. The computer system of claim 36 wherein each of the dummy loads comprises a circuit substantially identical to a respective one of the input receivers.

38. The computer system of claim 29 wherein each of the input receivers comprises a pair of differential transistors coupled to each other through a common node, and wherein each of the isolation circuits comprises a respective bias circuit operable responsive to a respective one of the activate signals to bias the differential transistors to a non-linear operating range.

39. The computer system of claim 38 wherein each of the bias circuits is coupled to the common node of the respective input receiver.

40. The computer system of claim 29 wherein each of the output signal detectors comprises a respective logic gate.

41. The computer system of claim 40 wherein the logic gate comprises a NOR gate.

42. A method of protecting a reference voltage source from noise generated by applying an output signal to an input/output terminal to which an input receiver is also coupled through a first input terminal of the input receiver, the input receiver further having a second input terminal to which the reference voltage source is coupled, the method comprising:

detecting when the output signal is being applied to the input/output terminal;

when the output terminal is not detected as being applied to the input/output terminal, coupling the reference voltage source to the input/output terminal through the input receiver; and

when the output terminal is detected as being applied to the input/output terminal, isolating the reference voltage source from the input/output terminal.

43. The method of claim 42 wherein the act of isolating the reference voltage source from the input/output terminal comprises isolating the reference voltage source from the second input terminal of the input receiver.

44. The method of claim 42 wherein the act of isolating the reference voltage source from the input/output terminal comprises isolating the first input terminal of the input receiver from the input/output terminal.

45. The method of claim 42 wherein the act of isolating the reference voltage source from the input/output terminal comprises biasing a node of the input receiver to a voltage that substantially reduces coupling from the first input terminal of the input receiver to the second input terminal of the input receiver.

46. The method of claim 45 wherein the input receiver comprises a first MOSFET transistor having a gate coupled to the first input terminal and a second NMOS transistor having a gate coupled to the second input terminal and a source coupled to a source of the first NMOS transistor, and wherein the act of biasing a node of the input receiver to a voltage that substantially reduces to coupling from the first input terminal of the input receiver to the second input terminal of the input receiver comprises coupling a bias voltage to the sources of the first and second NMOS transistors.

47. The method of claim 42, further comprising coupling the input/output terminal to a dummy load when the reference voltage source is being isolated from the input/output terminal.

48. The method of claim 42, further comprising maintaining the impedance at the input/output terminal substantially constant while switching between coupling the reference voltage source to the input/output terminal and isolating the reference voltage source from the input/output terminal.

49. In a memory device having a plurality of input/output terminal coupled to respective output drivers and to respective input receivers each of which is operable to compare an input signal applied to the input/output terminal to a reference voltage generated by a reference voltage source that is coupled to the input receivers for a plurality of the input/output terminals, the method comprising:

detecting when an output signal from a respective one of the output drivers is being coupled to each of the input/output terminals;

when an output signal from each of the output drivers is not detected, coupling the respective input/output terminal to the reference voltage source through the respective input receiver; and

when an output signal from each of the output drivers is detected, isolating the respective input/output terminal from the reference voltage source.

50. The method of claim 49 wherein the act of detecting when an output signal is being coupled to each of the input/output terminal comprises:

generating a respective enable signal from each of the output drivers indicative of the output driver being enabled; and

detecting each of the enable signals.

51. The method of claim 49 wherein the act of isolating the respective input/output terminal from the reference voltage source comprises isolating the reference voltage source from the input receiver.

52. The method of claim 49 wherein the act of isolating the respective input/output terminal from the reference voltage source comprises isolating the input receiver from the input/output terminal.

53. The method of claim 49 wherein the act of isolating the reference voltage source from the input/output terminal comprises biasing a node of the input receiver to a voltage that substantially reduces to coupling from a terminal of the input receiver that is coupled to the input/output terminal to a terminal of the input receiver that is coupled to the voltage reference source.

54. The method of claim 53 wherein each of the input receiver comprises a first MOSFET transistor having a gate coupled to a respective one of the input/output terminals and a second NMOS transistor having a gate coupled to the reference voltage source a source coupled to a source of the first NMOS transistor, and wherein the act of biasing a node of the input receiver to a voltage that substantially reduces to coupling comprises coupling a bias voltage to the sources of the first and second NMOS transistors.

55. The method of claim 49, further comprising coupling the input/output terminal to a dummy load when the reference voltage source is being isolated from the input/output terminal.

56. The method of claim 49, further comprising maintaining the impedance at the input/output terminal substantially constant while switching between coupling the reference voltage source to the input/output terminal and isolating the reference voltage source from the input/output terminal.